XCOM-6400

Intel® 4th Generation Core

COM Express CPU Module

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
Wixom, MI 48393-7037 U.S.A.
Tel: (248) 295-0310
Fax: (248) 624-9234

8501-003A

Table of Contents

1.0 GENERAL INFORMATION 5
1.1 Intended Audience 5
1.2 Preface 5
1.2.1 Trademark, Trade Name and Copyright Information 5
1.2.2 Class A Product Warning 5
1.2.3 Environmental Protection Statement 5
1.3 Product Summary 6
1.4 Related Material 6
1.5 Ordering Information 7
1.6 Key Features and Benefits 8
Fig. 1.6.a: XCOM-6400 Block Diagram 8
1.6.1 Intel® 4th Gen (Haswell) Core CPU 8
1.6.2 Intel QM87 Chipset (Lynx Point) PCH 9
1.6.3 Intel I217 PHY 10
1.6.4 Nuvoton NCT6776D Super-I/O 10
1.6.5 Atmel AT97SC3204 TPM 10
2.0 PREPARATION FOR USE 11
2.1 Unpacking and Inspecting 11
2.2 Carrier Board Considerations 12
2.3 Carrier Board Installation 12
2.4 Default Hardware Configuration 12
3.0 HARDWARE INFORMATION AND CONFIGURATION 13
3.1 Module Hardware Configuration 13
Table 3.1.a: Configuration Switches 13

3.2 Power Supply and Management 13
3.2.1 Power Options 13
3.2.2 Low Power Operation 14
3.2.3 Inrush Current 14
3.2.4 Power Management 14

3.3 CPU 15
3.3.1 Active Processor Core Selection 16

3.4 Platform Controller Hub (PCH) 16

3.5 System Memory 17

3.6 Video 17
3.6.1 Display Configuration and Resolution 17
Table 3.6.1.a: Valid Three Display Configuration through the Processor 18
3.6.2 PCI Express Graphics (PEG) 19
3.6.3 VGA 19
3.6.4 Digital Display Interfaces 19
3.6.5 Embedded DisplayPort 22
3.6.6 Configuring the Primary Display 22
3.6.7 Configuring the Video Memory 22
3.6.8 Video Display Options 22

3.7 Intel® High Definition Audio 22

3.8 Storage I/O 22
3.8.1 SATA 22

3.9 General I/O 23
3.9.1 General Purpose I/O (GPIO) 23
3.9.2 SMBus and I2C 23
Table 3.9.2.a: SMBus/I2C Address Table 23
3.9.3 Low Pin Count (LPC) 23
3.9.4 PCI Express 24
3.9.5 Serial Ports 24
3.9.6 SPI Flash 24
3.9.7 USB 25
3.9.7.1 Configuring USB Ports 25

3.10 Ethernet 25
3.10.1 Configuring Wake On LAN 26
3.10.2 Configuring PXE Boot 26

3.11 Real Time Clock (RTC) 26

3.12 Security 26
3.12.1 Trusted Platform Support 26
3.12.2 Password Control 26

3.13 System Management 27
3.13.1 Intel® Hyper-Threading Technology 27
3.13.2 Enhanced Intel® SpeedStep Technology (EIST) 27
3.13.3 Intel® Virtualization Technology (Intel VT-x and VT-d) 27
3.13.4 Intel® Trusted Execution Technology (TXT) 28
3.13.5 Intel® Turbo Boost Technology 28
3.13.6 Intel® Active Management Technology 29
3.13.7 Intel® Matrix Storage Technology 29
3.13.8 Intel® Configurable TDP Technology 29

3.14 Thermal Management 29
3.14.1 Fan Speed 30
3.14.2 Thermal Monitoring 30
3.14.3 Thermal Throttling 30
3.14.4 Memory Throttling 30
3.14.5 Thermal Management Hardware 30
Fig. 3.14.5.a XCOM-6400 without Thermal Management Hardware 31
Fig. 3.14.5.b XCOM-6400 and Heat Spreader 31
Fig. 3.14.5.c Module Mounting Screw Locations 32
Fig. 3.14.5.d SODIMM Assembly 33
Fig. 3.14.5.e XCOM-6400 with Heat Spreader and Active Heat Sink 34
Fig. 3.14.5.f XCOM-6400, ACEX-4620 Carrier Board, and Heat Spreader Assembly 34

3.15 Watchdog 35

4.0 BIOS INFORMATION AND CONFIGURATION 36

4.1 OS Support 36

4.2 Drivers and Utilities 36

5.0 SERVICE AND REPAIR 37

5.1 Service and Repair Assistance 37

5.2 Preliminary Service Procedure 37

5.3 Where to Get Help 37

6.0 SPECIFICATIONS 38

6.1 Physical **38**
6.1.1 J3 Connector 38
6.1.2 J4 Connector 38
6.2 Power Requirements **38**
6.3 Environmental Considerations **38**
6.4 Certificate of Volatility **40**
6.5 Revision History **40**
APPENDIX A: COM EXPRESS CONNECTOR (J4) PINOUT TABLES **41**

1.0 GENERAL INFORMATION

1.1 Intended Audience

This users' manual was written for technically qualified personnel who will be working with I/O devices using the XCOM-6400 CPU. It is not intended for a general, non-technical audience that is unfamiliar with computer-on-module (COM) devices and their application.

1.2 Preface

The information contained in this manual is subject to change without notice, and Acromag, Inc. (Acromag) does not guarantee its accuracy. Acromag makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Further, Acromag assumes no responsibility for any errors that may appear in this manual and makes no commitment to update, or keep current, the information contained in this manual. No part of this manual may be copied or reproduced in any form, without the prior written consent of Acromag,

1.2.1 Trademark, Trade Name and Copyright Information

1.2.2 Class A Product Warning

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may find it necessary to take adequate corrective measures.

1.2.3 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many components used (structural parts, circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposition of this product after its service life must be conducted in accordance with applicable country, state, or local laws or regulations.

1.3 Product Summary

COM Express™ is an open-industry standard for computer-on-modules (COMs). These are highly-integrated and compact PCs that can be used in a design application much like an integrated circuit component. Each COM Express module integrates core CPU and memory functionality, the common I/O of a PC/AT, USB, audio, graphics (PEG), and Ethernet. All I/O signals are mapped to two high density, low profile connectors on the bottom side of the module.

The XCOM-6400 uses an Intel® 4th Generation Core Processor (Haswell) module in a Type 6 COM Express basic form factor (125mm x 95mm). It fully conforms to Revision 2.1 of the COM Express Module Base Specification except as noted in Appendix A.

The module can support either one or two DDR3L ECC SODIMMs, for a total of up to 16GB. The SODIMMs are firmly attached to the module with screws and surrounded by heat sink material to provide a mechanically and thermally robust mechanism. Extended temperature models are available for operating in a -40°C to +85°C range (see Table 1 below).

A large amount of I/O is available, as summarized in the "Key Features and Benefits" section below.

A two digit LED display is available for Power ON Self Test (POST) codes, should a problem arise during the boot operation. This display is available for application software user codes after POST to aid in software debugging.

All functional I/O and input power are available on the COM-Express Connector (J4). In order for this module to function and to gain access to the I/O it must be installed in a Type 6 Com Express carrier board.

<u>Note:</u> Installation onto any carrier board other than a Type 6 could cause damage to this module and/or the carrier board!

A 26-pin XDP debug connector is available for connecting the emulator tools directly to the CPU.

1.4 Related Material

The following manuals and part specifications provide the necessary information for in-depth understanding of the XCOM-6400 module.

- COM-Express Module Base Specification Rev. 2.1 http://www.picmg.org
- The Haswell Core BIOS Manual
- Intel® document No. 328901, "Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2", Rev: 002; September, 2013. http://www.intel.com/content/www/us/en/processors/core/CoreTechnicalResources.html
- XCOM-6400 Engineering Design Kit (EDK)

1.5 Ordering Information

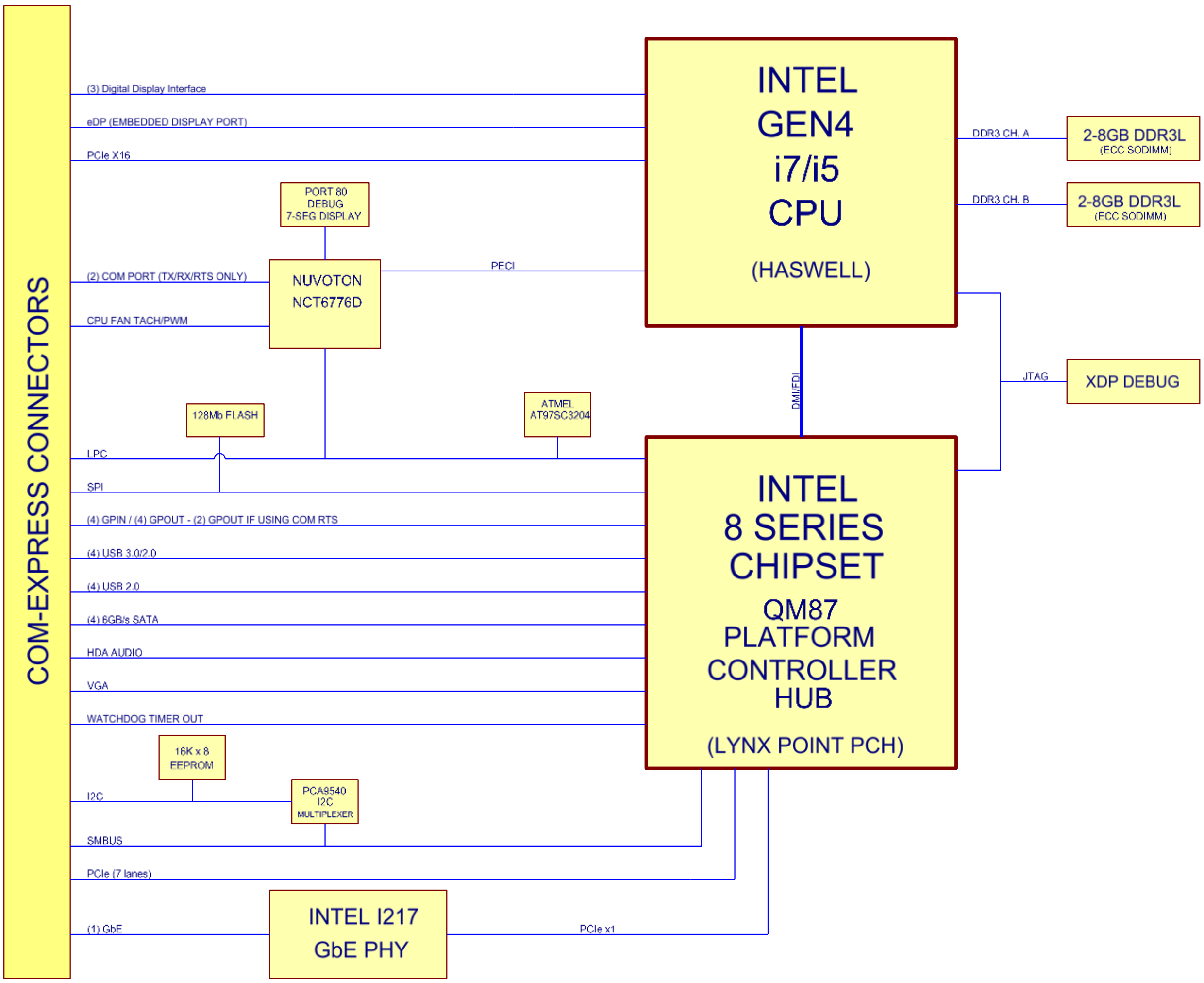
When ordering the XCOM-6400-ABBD-X COM Express module, please select from and specify the available option choices (A, BB, D and X) as defined below (such as XCOM-6400-116E-L, XCOM-6400-304L-F, etc.):

- Select the CPU option (A):
  - ✓ 1: i7-4770EQ, 2.4GHz, quad core, 6Mb Cache
  - ✓ 3: i5-4402E, 1.6GHz, dual core, 3Mb Cache
- Select the memory option (B);
  - ✓ 04: 4Gb
  - ✓ 08: 8Gb
  - ✓ 16: 16Gb
- Select the operating environment (temperature) option (D):
  - ✓ Blank: Standard temperature operation
  - ✓ E: Extended temperature operation
- Select the solder option (X):
  - ✓ L: Lead solder
  - ✓ LF: Lead-free solder

1.6 Key Features and Benefits

The XCOM-6400 block diagram shown in Fig. 1.6.1 illustrates the key components and features that are summarized on the following pages.

Fig. 1.6.a: XCOM-6400 Block Diagram



1.6.1 Intel® 4th Gen (Haswell) Core CPU

Available as either a 2.4GHz quad-core i7 or a 1.6GHZ dual-core i5. This 64-bit, 22-nanometer (Haswell) CPU with integrated GT2 graphics contains direct interfaces for DDR3L, DDI, and PCIe x16, all of which are available on the COM Express connector. In addition, the Direct Media Interface (DMI) is used to connect to the QM87 Platform Control Hub (PCH).

- **DDR3L SDRAM –** Two SODIMM sockets support up to 16GB of DDR3L ECC at 1600MHz. Dual-channel mode is used with the two SODIMMs. The SODIMMs are attached to the module firmly with screws and surrounded by heat sink material to provide a robust mechanism both mechanically and thermally.

- **PCIe x16 –** Traditionally used for external graphics, but supports any PCIe device(s). Can also be split into two x8 interfaces or one x8 and two x4 interfaces.
- **DDI (3) –** These Digital Display Interfaces can be configured to be Displayport 1.2, DVI, or HDMI.
- **eDP –** Embedded DisplayPort allows direct connection to a display panel using up to two lanes for communication. Backlight and voltage enable lines are also available.

1.6.2 Intel QM87 Chipset (Lynx Point) PCH

The Intel 8 Series QM87 (Lynx Point) PCH provides extensive I/O support, all of which is available on the COM-EXPRESS connector and is listed below:

- **PCIe (7)** – There are seven lanes of PCIe available in addition to the x16 from the CPU.
- **SATA III (4)** – There are four SATA ports that operate up to 6Gb/sec.
- **USB 3.0 (4)** – There are four ports available that support USB 3.0 speed. These ports are backwards compatible to USB 2.0 and USB 1.1.
- **USB 2.0 (4)** – There are four additional ports that function at USB 2.0 or USB 1.1 speeds.
- **VGA** – An analog VGA port is available, including DDC clock and data.
- **GPIN (4) –** There are four 3.3V general purpose inputs available. Do not exceed 3.6V or the module may be damaged.
- **GPOUT (4) –** There are up to four 3.3V general purpose outputs available.
- **WDTO** – This Watchdog Timer Output indicates a watchdog time-out event has occurred. This output remains high until cleared by module software.
- **LPC –** Low Pin Count bus allows connection of slower devices on the carrier, typically Super-I/O or TPM devices.
- **SPI –** The Serial Peripheral Interface is used for the onboard boot flash. This interface is available on the carrier for connection of other user flash devices. Note that booting from carrier SPI is not supported by the module.
- **HDA Audio** – The HDA audio port is available to compatible CODECs on the carrier.
- **I2C** – This I2C bus is available for general user devices. It also contains an onboard EEPROM for module identification. Note that to access this bus from the PCH the connection must first be enabled in the PCA9540 (see below).
- **SMBUS** – This I2C-compatible System Management Bus is available to the carrier, but care should be taken not to interfere with any devices on the module.

1.6.3 Intel I217 PHY

The Intel I217 is a single-port Gigabit Ethernet Physical Layer Transceiver (PHY). It connects to the PCH's integrated Media Access Controller (MAC) through a dedicated interconnect. It supports 10/100/1000 Mb/s data rates and is available on the COM-Express connector.

1.6.4 Nuvoton NCT6776D Super-I/O

The Nuvoton NCT6776D is an LPC device that provides temperature and voltage monitoring, Port 80 debug via 2 digit 7-segment display, and the following signals available on the COM-Express connector:

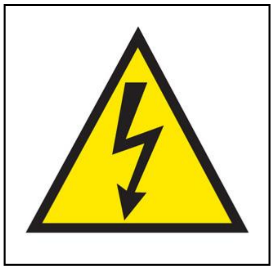
- **Serial Port (2) –** 2 16550-compatible serial ports (TX/RX/RTS only).
- **CPU Fan Tach/PWM –** Supplies PWM signal for fan control and receives tach output from fan for speed monitoring.

1.6.5 Atmel AT97SC3204 TPM

The Atmel AT97SC3204 is a fully integrated security module that implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM). The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

2.0 PREPARATION FOR USE

IMPORTANT PERSONAL AND PRODUCT SAFETY CONSIDERATIONS



It is very important for the user to consider the possible safety implications of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where personal injury or the loss of economic property or human life is possible. It is important that the user employ satisfactory overall system design. It is understood and agreed by the Buyer and Acromag that this is the Buyer's responsibility.



WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation. This product is an electrostatic sensitive device and is packaged accordingly. Do not open or handle this product except at an electrostatic-free workstation. Additionally, do not ship or store this product near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer’s packaging. Be aware that failure to comply with these guidelines will void the Acromag Limited Warranty.

2.1 Unpacking and Inspecting

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

2.2 Carrier Board Considerations

Refer to the specifications section for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

In an air cooled assembly, the optional active heatsink must be used and adequate air circulation must be provided to prevent a temperature rise above the maximum operating. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

In a conduction cooled assembly, adequate thermo conduction must be provided to prevent a temperature rise above the maximum operating temperature.

2.3 Carrier Board Installation

Remove power from the system before installing the carrier board.

2.4 Default Hardware Configuration

If necessary, the XCOM Express module may be configured differently than as received, depending on the application. When the module is shipped from the factory, it is configured as follows:

- PEG port configuration: 2 x8 ports. For information on reconfiguring the PEG port see Section 3.2, "Module Hardware Configuration."
- PCIE port configuration: PCIE(0:3): x4, PCIE4: x1, PCIE5: x1, PCIE6: x1; For information on reconfiguring the PCIE ports see Section 4.0, "BIOS Information and Configuration."

3.0 HARDWARE INFORMATION AND CONFIGURATION

3.1 Module Hardware Configuration

Table 3.1.a summarizes the functions, settings, and descriptions for switches SW-1 and SW-2.

Table 3.1.a: Configuration Switches

Configuration Switches			
Position	**Function**	**Switch Setting**	**Description**
1:2	PEG Port Bifurcation/ Trifurcation	OFF:OFF	PEG is 1 x 16
		OFF:ON	PEG is 2 x 8
		ON:OFF	Reserved
		ON:ON	PEG is 1 x8, 2 x4
3	ME RTC Reset	OFF	Normal Operation
		ON	Clears ME
4	BIOS/PCH RTC Reset	OFF	Normal Operation
		ON	Clears BIOS/RTC

SW1-1 and SW1-2 control PEG port Bifurcation: The PEG port can be configured as:

- a single x16 port, two x8 ports, or
- 1 x8 port and two x4 ports. In this last case the x8 port uses lanes 0-7, the first x4 port uses lanes 8-11, and the second x4 port uses lanes 12-15.

SW1-3 is used to clear the PCH Management Engine (ME) settings. To clear these settings, close the switch and then open it again.

Note: After clearing the ME settings, the RTC settings must also be cleared by closing SW1-4 and opening it again. If SW1-4 is not closed and reopened AFTER opening SW1-3, the module will not boot.

SW1-4 is used to clear the BIOS setup configuration as well as internal PCH registers connected to the RTC voltage. To clear these settings, close the switch and then open it again before use. Note that leaving the board unplugged from a carrier that supplies the RTC voltage for more than one hour will also clear these settings.

3.2 Power Supply and Management

3.2.1 Power Options

When using the Acromag ACEX-4610/20 carrier board, the carrier provides a 12V plus 5V standby power supply to the system module.

When using a carrier board other than the ACEX-4610/20, the module can be powered from either the 12V only, or 12V plus 5V standby power

source.

<u>Note</u>: Installation onto any carrier board other than a Type 6 could cause damage to this module and/or the carrier board, and is not recommended!

3.2.2 Low Power Operation

Applications requiring less power can reduce power consumption by disabling one or more of the CPU cores that are not required for running the application. The number of active CPU cores can be specified in the CPU configuration menu. However, Acromag recommends keeping all of the CPU cores active in high-performance systems requiring all available computing power.

Additional suggestions for reducing power consumption include making the following changes to the BIOS configuration:

- Disable unnecessary interfaces that require large amounts of power
- Use power-saving algorithms.
- Reduce the input voltage and processor frequency to the lowest allowable levels by using the available Intel SpeedStep® feature.

3.2.3 Inrush Current

This material is still under development.

3.2.4 Power Management

The XCOM-6400 module uses the Advanced Configuration and Power Interface (ACPI) 3.0 standard to provide user-managed power via the operating system, contingent upon the carrier board selected.

3.2.4.1 ACPI System States

The five ACPI “Supported Module States” are described as follows:

- G0/S0: Fully operational; the main memory is being used for all work.
- S3: Standby; the main memory is still powered up, but the work is suspended to RAM. Work will be resumed exactly where it was stopped when standby was initiated.
- S4 — Hibernate; all work and content residing in the main memory is saved to a non-volatile memory media, and the main memory is then powered down.
- S5: Soft off. Power is removed from all devices, including the main memory, RAM, and all volatile memory devices. This results in all memory content being lost.
- G3: Unpowered. Power has been mechanically removed from the system. Wake-up is not possible in this state.

Note that all of these states are supported with the Acromag ACEX-4610/20 carrier boards but may not be with other carriers. An ACPI-aware operating system must be installed and either 5V Standby or 12V must remain applied to

the module at all times for S3, S4, or S5 support.

3.2.4.2 APCI Wake-Up Events

The XCOM-6400 module supports the following wake-up events from the S3, S4, and S5 power states if 12V operating power or 5V standby power are provided by the power supply:

- Power button
- Wake On LAN (instructions can be found in Sub-section 3.10.1, “Configuring Wake On LAN”).
- RTC alarm (instructions can be found in Sub-section 3.11, “Real Time Clock (RTC)”.
- PCI and PCI Express power management event signaling; PME wake-up is enabled by default.

3.2.4.3 APCI Processor States

The Advanced Configuration and Power Interface (ACPI) provides an open standard for device configuration and power management by the operating system. More details about this feature are provided in *The Haswell Core BIOS Manual*.

3.3 CPU

The Intel® Gen 4 (Haswell) CPU is available as either a 2.4GHz quad-core i7 or a 1.6GHZ dual-core i5. This 64-bit, 22-nanometer CPU with integrated GT2 graphics contains direct interfaces for DDR3L, DDI, and PCIe x16, all of which are available on the COM-Express connector. In addition, the Direct Media Interface (DMI) is used to connect to the QM87 Platform Control Hub (PCH).

- **DDR3L SDRAM –** 2 SODIMM sockets support up to 16GB of DDR3L ECC at 1600MHz. Dual-channel mode is used with 2 SODIMMs. The SODIMMs are attached to the module firmly with screws and surrounded by heat sink material to provide a robust mechanism both mechanically and thermally.
- **PCIe x16 –** This is traditionally used for external graphics, but supports any PCIe device(s). It can also be split into 2 x8 interfaces or 1 x8 and 2 x4 interfaces, as selected by SW1-1 and SW1-2. See Section 3.2, “Module Hardware Configuration.”
- **DDI (3) –** These Digital Display Interfaces can be configured to be Displayport 1.2, DVI, or HDMI. Three simultaneous displays are possible. See Section 3.7.1, “Display Configuration and Resolution”, for a list of valid combinations.
- **eDP –** The embedded DisplayPort allows direct connection to a display panel using up to two lanes for communication. Backlight and voltage enable lines are also available, and up to two other simultaneous displays are possible. See Section 3.7.1, “Display Configuration and Resolution”, for a list of valid combinations.

3.3.1 Active Processor Core Selection

All of the CPU cores should be kept active in high-performance systems requiring all available computing power. Conversely, applications having reduced power requirements can save power by disabling one or more of the CPU cores. The number of active CPU cores can be specified in the CPU configuration menu.

3.4 Platform Controller Hub (PCH)

The Intel 8 Series QM87 Lynx Point PCH provides extensive I/O support, all of which is available on the COM-EXPRESS connector and is listed below:

- **PCIe (7)** – There are seven lanes of PCIe available in addition to the x16 from the CPU. These lanes are configured by default as x4, x1, x1, x1 but can be reconfigured to other port/lane widths using the XCOM-6400 PCI Express configuration tool.
- **SATA III (4)** – There are four SATA ports that operate up to 6Gb/sec.
- **USB 3.0 (4)** – There are four ports available that support USB 3.0 speed. These ports are backwards compatible to USB 2.0 and USB 1.1.
- **USB 2.0 (4)** – There are four additional ports that function at USB 2.0 or USB 1.1 speeds.
- **VGA** – An analog VGA port is available, including DDC clock and data. Three simultaneous displays are possible. See Section 3.7.1, "Display Configuration and Resolution", for a list of valid combinations.
- **GPIN (4) –** There are four 3.3V general purpose inputs available. Do not exceed 3.6V or the module may be damaged. See Section 3.9.1, "General Purpose I/O (GPIO)", for more information.
- **GPOUT (4) –** There are up to four 3.3V general purpose outputs available. See Section 3.9.1, "General Purpose I/O (GPIO)", for more information.
- **WDTO** – This Watchdog Timer Output indicates a watchdog time-out event has occurred. This output remains high until cleared by module software.
- **LPC –** Low Pin Count bus allows connection of slower devices on the carrier, typically Super-I/O or TPM devices.
- **SPI –** The Serial Peripheral Interface is used for the onboard boot flash. This interface is available on the carrier for connection of other user flash devices. Note that booting from carrier SPI is not supported by the module.
- **HDA Audio** – The HDA audio port is available to compatible CODECs on the carrier.
- **I2C** – This I2C bus is available for general user devices. It also contains an onboard EEPROM for module identification. Note that to access this bus from the PCH the connection must first be enabled in the PCA9540 (see below).

- **SMBUS** – This I2C-compatible System Management Bus is available to the carrier, but care should be taken not to interfere with any devices on the module.

3.5 System Memory

XCOM-6400 COM Express modules have two 204-pin, right-angle SO-DIMM sockets (J1, J2) to accept DDR3L ECC SDRAM modules. At least one SDRAM module is required to make the system operational. Note that ECC (x72) SODIMM modules are required. Non-ECC modules (x64) are not supported.

Support for the following features is provided by the system memory interface:

- DDR3 SDRAM with transfer rates of 1600 MT/s
- 1 GB, 2 GB, 4 GB, and 8 GB DDR3 SDRAM densities
- 72-bit wide channels (64-bits plus 8 bits of ECC)

3.6 Video

3.6.1 Display Configuration and Resolution

(The information and table shown below are from Intel® document No. 328901, "Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2", Rev: 002; September, 2013.)

The processor's digital ports can be configured to support DisplayPort*/HDMI/DVI. Table 3.6.1.a below shows examples of valid three display configurations and resolutions that are available with the Intel® 4th Gen (Haswell) Core CPU.

Table 3.6.1.a: Valid Three Display Configuration through the Processor

			Maximum Display Resolution		
Display 1	**Display 2**	**Display 3**	**Display 1**	**Display 2**	**Display 3**
HDMI	HDMI	DP	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz		3840x2160 @ 60 Hz
DVI	DVI	DP	1920x1200 @ 60 Hz		3840x2160 @ 60 Hz
DP	DP	DP	3840x2160 @ 60 Hz		
VGA	DP	HDMI	1920x1200 @ 60 Hz	3840x2160 @ 60 Hz	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz
eDPx2	DP	HDMI	2880x1800 @ 60 Hz		4096x2304 @ 24 Hz 2560x1600 @ 60 Hz
eDPx2	DP	DP	2880X1800 @ 60 Hz	3840x2160 @ 60Hz	
eDPx2	HDMI	HDMI	2880x1800 @ 60 Hz	4096x2304 @ 24 Hz 2560x1600 @ 60 Hz	

Notes:

1. Requires support of two channel DDR3L/DDR3L-RS 1600 MT/s configuration for driving three simultaneous 3840x2160 @ 60 Hz display resolutions

2. DP resolutions in the above table are supported for four lanes with link data rate HBR2.

Any 3 displays can be supported simultaneously using the following rules:

- Max of 2 HDMIs
- Max of 2 DVIs
- Max of 1 HDMI and 1 DVI
- Any 3 DisplayPort
- One VGA
- One eDP

3.6.2 PCI Express Graphics (PEG)

The PEG interface connects the Intel®4th Gen (Haswell) processor to PCI Express lanes [16:31] on the COM Express connectors.

The PEG interface meets the *PCI Express Base Specification, Revision 3.0* and supports:

- Low Swing (low-power/low-voltage) and Full Swing operating modes
- Static lane numbering reversal
- The Gen3 (8 GT/s) PCI Express frequency

3.6.2.1 Configuring the PEG

PEG configuration details and combinations are provided in Section 3.1, "Module Hardware Configuration."

3.6.2.2 Configuring the PEG Lanes

The PEG lane usage is configured using switches SW1-1 and SW1-2. See Section 3.1, "Module Hardware Configuration." and Table 3.1.a, "Configuration Switches", for further information regarding these switches and their configuration.

3.6.3 VGA

The XCOM-6400 COM Express module uses the Intel® Lynx Point controller to support the analog VGA interface

The VGA interface features include:

- Integrated 180 Mhz 24-bit RAMDAC
- Support for analog monitor resolutions up to 1920x2000 @60 Hz

3.6.4 Digital Display Interfaces

The Intel® Gen4 (Haswell) CPUused in the XCOM-6400 COM Express module integrates three digital display ports (B, C, and D), with each port supporting one of the following carrier board interfaces:

- Port B (DDI 1) supports DisplayPort, HDMI or DVI
- Port C (DDI 2) supports DisplayPort, HDMI or DVI
- Port D (DDI 3) supports DisplayPort, HDMI or DVI

DisplayPort can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and the link data rate of the RBR (1.62 GT/s), HBR (2.7 GT/s), and HBR2 (5.4 GT/s).

When configured as HDMI, the DDIx4 port can support 2.97 GT/s. Each digital port can drive resolutions of up to:

- 3840x2160 at 60Hz using DisplayPort ,
- 4096x2304 at 24 Hz/2560x1600 at 60Hz using single-link HDMI, and
- 1920x1200 at 60Hz using single-link DVI.

The processor supports High-bandwidth Digital Content Protection (HDCP) for high-definition content playback over digital interfaces.

The processor also integrates a dedicated Mini HD audio controller to drive audio on integrated digital display interfaces, such as HDMI* and DisplayPort*. The HD audio controller on the PCH would continue to support down CODECs, and so on. The processor Mini HD audio controller supports two High-Definition Audio streams simultaneously on any of the three digital ports.

The processor supports streaming any 3 independent and simultaneous display combination of DisplayPort*/HDMI*/DVI/eDP*/VGA monitors with the exception of three simultaneous display support of HDMI*/DVI . In the case of three simultaneous displays, two High Definition Audio streams over the digital display interfaces are supported.

3.6.4.1 DisplayPort

DisplayPort (DP) is a VESA standard-based specification that provides a large bandwidth bus interface for connections between computers and their displays. By using differential signaling to combine internal and external connection methods, DP reduces device complexity, supports cross-industry applications, and provides performance scalability. In addition to applications using monitors, television sets, and projectors, DPcan also be used with a variety of consumer electronic products (such as high-definition optical disc players and set-top boxes), and will enable the next generation of display devices.

The BIOS will automatically detect installed devices that are using DP interfaces, and configure those devices according to the video BIOS settings. For further information regarding BIOS device configuration BIOS, refer to Section 4.0, “BIOS Information and Configuration.

The Intel® 4th Gen Haswell Core CPU can support a maximum of three DP ports simultaneously.

3.6.4.2 DVI

A Digital Visual Interface (DVI) transmits uncompressed digital audio and video signals from AV sources to video display devices. The DVI interface originates from the CPU, and supports DVI-D (digital only),

The DVI interface utilizes transition minimized differential signaling (TMDS) to transmit audio, video and auxiliary (control/status) data information through the DVI cable.

The BIOS will automatically detect installed devices that are using DVI interfaces, and will automatically configure the installed devices according to the video BIOS settings. For further information regarding BIOS device configuration BIOS, refer to Section 4.0, “BIOS Information and Configuration.

3.6.4.3 HDMI

(The information below is from Intel® document No. 328901, "Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 of 2", Rev: 002; September, 2013.)

The High-Definition Multimedia Interface* (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audiovisual sources to television sets, projectors, and other video displays. It can carry high quality multi-channel audio data, and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. The HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface with 3D, 4K, Deep Color, and x.v.Color.

3.6.4.4 Integrated Audio

(The information below is from Intel® document No. 328901, "Mobile 4th Generation Intel® Core™ Processor Family Datasheet – Volume 1 2", Rev: 002; September, 2013.)

HDMI and display port interfaces carry audio along with video.

- The processor supports two DMA controllers to output two high definition audio streams on two digital ports simultaneously.
- The processor supports only the internal HDMI and DP CODECs.

The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI and DisplayPort monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2

kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

3.6.5 Embedded DisplayPort

A dedicated embedded DisplayPort (eDP) interface is included in the XCOM-6400 module, which supports link speeds of 1.62 Gbps and 2.7 Gbps link speeds on 1 or 2 data lanes.

3.6.6 Configuring the Primary Display

To select a specific primary display, refer to *The Haswell Core BIOS Manual.*

3.6.7 Configuring the Video Memory

To configure the video memory, refer to *The Haswell Core BIOS Manual.*

3.6.8 Video Display Options

The COM Express module supports up to three independent displays using the rules given in Section 3.6.1, "Display Configuration and Resolution." An external GPU add-in card can be installed in the PEG port(s) to add additional display ports.

Display mode choices when using multiple monitors include:

- Single display, in which one port is activated to display the output on one device.
- Clone mode, in which the same content, resolution, and color depth are sent to up to three display devices. Different refresh rates may be used on each display.
- Extended desktop, in which a larger Windows desktop spans up to three display devices. The displays can support different refresh rates, resolutions, and color depth.

3.7 Intel® High Definition Audio

Up to four CODECs can be attached to the digital Intel® High Definition Audio (HDA) interface.

The module can also generate a separate PC speaker signal, although most CODECs intercept this signal and pipe it out through the speakers attached to the CODEC. Enabling and configuring the HDA is discussed in *The Haswell Core BIOS Manual.*

3.8 Storage I/O

3.8.1 SATA

SATA (Serial Advance Technology Attachment) is the interface that connects the PCH to the supported mass storage devices (see below). Independent operation is achieved with the two integrated SATA host controllers on the PCH using the four SATA 3.0 ports.

The SATA features support:

- The SATA hard disk drives, solid state drives (SSD), and

CD-ROM/DVD-ROM drives
- IDE, AHCI, and RAID (0, 1, 5, and 10) modes
- Data transfer rates of up to 6.0Gbps

To disable SATA operation, refer to *The Haswell Core BIOS Manual.*

3.9 General I/O

3.9.1 General Purpose I/O (GPIO)

The module PCH supports four GPIs [0:3] and four GPOs [0:3].

The GPINs are 3.3V level signals. Voltage exceeding 3.6V may damage the module. These are unbuffered on the module, so a buffer on the carrier is recommended.

The GPOUTs are also unbuffered and not intended as high current outputs. Buffering on the carrier is recommended as well.

GPOUT2 and GPOUT3 may be configured to be COM1 and COM2 RTS, respectively instead of general purpose IO's. This is required if these COM ports will use the RS422 or RS485 protocols. For configuration information see Section 4.0 BIOS Configuration.

3.9.2 SMBus and I2C

The carrier board is supplied with both SMBus and I2C buses. The SMBus is connected directly to the PCH, and the I2C bus is isolated using a PCA9540 I2C Multiplexer. Refer below to Table 3.9.2.a, SMBus/I2C Address Table, below for additional information.

Table 3.9.2.a: SMBus/I2C Address Table

SMBus/I2C ADDRESS TABLE		
BUS	SMBus ADDR	FUNCTION
SMB	0x32	DIMMA TEMP
SMB	0x34	DIMMB TEMP
SMB	0x5A	SUPER-I/O
SMB	0xA2	DIMMA SPD
SMB	0xA4	DIMMB SPD
SMB/I2C	0xE0	PCA9540B (TO CARRIER)
I2C	0xA0	COM-EXP ID EEPROM
SML0	0xC8	GbE PHY
SML0	0xE0	GbE MAC

3.9.3 Low Pin Count (LPC)

The LPC interface provided by the module complies with the LPC 1.1 Specification and supports two master/DMA devices, and allows for the connection of devices such as Super I/O, micro controllers, and customer ASICs.

The onboard NCT6776D Super I/O device supplies the two serial ports and also outputs the Port80 Power On Self Test (POST) codes to the dual 7-segment display DSI.

Since the NCT6776D uses DRQ0#, any additional LPC devices on the carrier must use DRQ1#.

For further information regarding the system BIOS and LPC interfaces, refer to *The Haswell Core BIOS Manual.*

3.9.4 PCI Express

Seven PCI Express port lanes [0:6] are available. Each port:

- Supports 5GBps bandwidth in each direction and
- Is compliant with PCI Express Base Specification Version 2.0.

3.9.4.1 Configuring Link Options for PCI Express Expansion Ports

PCI Express lanes [0:6] can be configured into different numbers of ports and witdths.

- Lanes [0:3] are by default configured as a single x4 port. Alternately, these lanes can be configured as :
  - ✓ 2 x2 ports (0&1, 2&3),
  - ✓ 1 x2 port + 2 x1 ports (0&1, 2, 3), or
  - ✓ 2 x1 ports + 1 x2 port (0, 1, 2&3)
- Lanes [4:5] by default are configured as 2 x1 ports. Alternately, they can be configured as a single x2 interface.
- Lane 6 is set as a one x1 interface, and must remain as such.

The XCOM-6400 PCI Express Configuration tool can be used to reconfigure any valid combination of port/lane widths.

3.9.5 Serial Ports

Two 16550-compatible serial ports are supported by the NCT6776 Super I/O chip, with the signals being sent to board-to-board interconnections.

For further information regarding BIOS serial port configuration, refer to *The Haswell Core BIOS Manual.*

3.9.6 SPI Flash

The Intel® Lynx Point PCH chipset supports SPI-compatible flash devices of up to 16MB flash ROM with two SPI chip-select signals, SPI_CS[0:1]#. Either SPI0 or SPI1 may provide the SPI source.

- One 16MB SPI flash is soldered onto the module and contains the BIOS firmware code.
- When the carrier board contains an SPI flash chip, this device can only be used for user storage.
- The system cannot be booted from the BIOS ROM on the carrier board.

Two boot BIOS selection straps, BIOS_DIS[0:1]#, are ignored and not supported by the XCOM-6400 module.

3.9.6.1 Supplying power to the carrier SPI

The SPI_POWER pin on theCOM Express connectors supplies a nominal 3.3V suspend/3.3V, 100mA to the SPI bus on the carrier board. The carrier board must use less than 100mA of SPI_POWER.

Note: To avoid the possibility of power rail leakage or other incompatibilities:

- The carrier board must use SPI_POWER from the COM Express module to supply the power to the carrier board's SPI bus, and
- SPI_POWER must only be used to power SPI devices on the carrier board.

3.9.7 USB

The Intel® Lynx Point PCH has up to two Enhanced Host Controller Interface (EHCI) host controllers to support USB high-speed signaling on all eight USB 2.0 high-speed ports (USB 2.0 allows data transfers up to 480 Mbps.).

The Intel® Lynx Point PCH also has an eXtensible Host Controller Interface (xHCI) host controller to support four USB 3.0 ports. This allows data transfers of up to 5 Gbps, which is 10 times faster than high-speed USB 2.0.

These USB features support:

- USB hard disk drives, flash drives, floppy disk drives, and CD-ROM/DVD-ROM drives
- Super-speed, high-speed, full-speed, and low-speed USB
- USB 3.0 Super-speed on four of eight USB 2.0 expansion ports
- High-speed USB 2.0 debug port on USB port 1
- Console redirection on USB port 1 with a debug cable

PCH USB 2.0 ports 0, 1, 2, 3, 8, 9, 10, and 11 are routed through the board-to-board connector USB [0:7].

- PCH USB 3.0 ports 1,2,5, and 6 are routed through the board-to-board connector USB_SS[0:3]

3.9.7.1 Configuring USB Ports

For information on configuring specific USB ports see *The Haswell Core BIOS Manual.*

3.10 Ethernet

The XCOM-6400 module uses the Intel® Lynx Point PCH's integrated Gigabit Ethernet controller along with the i217 Ethernet PHY to support one 10/100/1000 Mbps Ethernet interface.

Ethernet features include:

- Gigabit Ethernet support via the PCI Express x1 interface
- 10/100/1000 Mbps full-duplex and half-duplex operation
- IEEE 802.3x-compliant flow control support with software

controllable pause times and threshold values

- IEEE802.3ab auto-negotiation support and IEEE802.3ab PHY compatibility
- Full wake-up support
- Programmable LEDs for traffic, a 100Mbps link, and a 1000Mbps link.
  - ✓ The Link# signal on the board-to-board connectors is the 100Mbps and 1000Mbps link signals added together.
  - ✓ When using a 10Mbps link, one of these LEDs must be reprogrammed to be a generic link in order for the link status to be displayed on the Link# output.

3.10.1 Configuring Wake On LAN

This material is still under development

3.10.2 Configuring PXE Boot

For information regarding how to boot from the network,, refer to *The Haswell Core BIOS Manual.*

3.11 Real Time Clock (RTC)

A Motorola® MS146818B-compatible real-time clock (RTC) is included in the Intel® Lynx Point PCH. The RTC has 256 bytes of battery-backed RAM and runs on a 32.768 KHz crystal with a 3V battery. The RTC performs two key functions:

- It keeps track of the time of day, and
- It stores system data, even after powering down the system.

Note: After the RTC battery is removed from the carrier board, the last BIOS settings will be retained for approximately 60 minutes by an onboard superCap. After that, the settings will be lost unless the module is reconnected to a carrier containing a 3V RTC battery voltage.

3.12 Security

3.12.1 Trusted Platform Support

The XCOM-6400 uses the Atmel AT97SC3204 fully integrated security module, which implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM). The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

3.12.2 Password Control

You are able to specify:

- An Administrator password with full control, and
- A User password with limited access to the BIOS settings.

For further information on setting the password, refer to *The Haswell Core BIOS Manual.*

3.13 System Management

3.13.1 Intel® Hyper-Threading Technology

(Note: The following information is from Intel® publication "External Design Specifications – Volume 1 of 2" for the 4th Generation Intel® Core™ Processor.)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

The Intel® HT Technology is enabled by default; no action by the operator is required.

For further information on disabling support for this technology, refer to *The Haswell Core BIOS manual.*

3.13.2 Enhanced Intel® SpeedStep Technology (EIST)

The Enhanced Intel® SpeedStep Technology (EIST) used by this processor enables very high performance while also meeting power-conservation needs. When EIST is enabled, the clock frequency of the CPU is dynamically changed in response to the CPU load

The Intel® SpeedStep feature is enabled by default. For further information on disabling support for this technology, refer to *The Haswell Core BIOS Manual.*

3.13.3 Intel® Virtualization Technology (Intel VT-x and VT-d)

Intel® Virtualization Technology (Intel VT) makes a single system appear as multiple independent systems to software. This allows for multiple, independent operating systems to be running simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. The first revision of this technology (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. The second revision of this specification (Intel VT-d) adds chipset hardware implementation to improve I/O performance and robustness.

The Intel® VT-x and VT-d features are enabled by default. For further information on disabling support for this technology, refer to *The Haswell Core BIOS Manual.*

3.13.4 Intel® Trusted Execution Technology (TXT)

The featured Intel® Trusted Execution Technology attests to the authenticity of a platform and its operating system and assures that an authentic OS starts in a trusted environment and can be considered a trusted OS.

Intel® TXT works in conjunction with the TPM so that the system software may make trust decisions.

The Intel TXT feature is enabled by default. For further information on disabling support for this technology, refer to *The Haswell Core BIOS Manual.*

3.13.5 Intel® Turbo Boost Technology

The number of active cores determines the maximum processor core operating frequency. See Section 3.3.1, "Active Processor Core Selection" for information and instructions.

(Note: The following information is from Intel® publication "External Design Specifications – Volume 1 of 2" for the 4th Generation Intel® Core™ Processor)

The Intel® Turbo Boost Technology allows the processor core to opportunistically and automatically run faster than its rated operating frequency/render clock if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads.

The processor supports a Turbo mode in which the processor can use the thermal capacity associated with the package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, surging usage conditions. The turbo feature needs to be properly enabled by BIOS for the processor to operate with maximum performance. See the appropriate processor family BIOS writer's guide for enabling details. Since the turbo feature is configurable and dependent on many platform design limits outside of the processor control, the maximum performance cannot be ensured.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design.

Compared with previous generation products, Intel Turbo Boost Technology will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Refer to *The Haswell Core BIOS Manual* and the appropriate processor

Turbo Implementation Guide for more information.

3.13.6 Intel® Active Management Technology

(Note: The following information is from Intel® publication "External Design Specifications – April 2013, Revision 2.1" for the Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub [PCH]).

Intel® Active Management Technology (Intel® AMT) is a set of advanced manageability features developed to extend the manageability capability for IT through Out Of Band (OOB). This allows asset information, remote diagnostics, recovery, and contain capabilities to be available on client systems even when they are in a low power, or "off" state, or in situations when the operating system is hung.

For further information on configuring this technology, refer to *The Haswell Core BIOS Manual.*

3.13.7 Intel® Matrix Storage Technology

Intel® Matrix Storage Technology is supported by Intel's 8 Series QM87 Lynx Point PCH, which provides:

- AHCI functionality,
- RAID 0/1/5/10 Support, and
- Intel® Smart Response Technology.

3.13.8 Intel® Configurable TDP Technology

Intel® Configurable TDP Technology (cTDP) allows users to reconfigure the 47W thermal design power (TDP) level of the i7-4700EQ CPU down to 37W in systems where a lower amount of power is available or a smaller thermal solution is required.

For further information on configuring the TDP levels, refer to The Haswell Core BIOS Manual.

3.14 Thermal Management

The Intel® Haswell processor contains a digital thermal sensor for each execution core and a thermal monitor to measure the processor's temperature. A thermal sensor connected to the NCT6776 Super-I/O is used to measure the module's temperature.

The integrated graphics and memory controller (GMC) monitors its temperature and initiates thermal management with an internal digital thermal sensor. Memory loading or high GMC temperatures will result in bandwidth throttling. THERMTRIP# and Render Thermal Throttling are also supported by the internal digital thermal sensor.

The temperature of the Intel® Lynx Point PCH is monitored by two thermal sensors located on the PCH. The system will be shut down by the PCH when its thermal limit is reached.

3.14.1 Fan Speed

The CPU fan is monitored and controlled by the Nuvoton NCT6776D LPC device. It receives a tachometer output from the CPU fan for speed monitoring, and provides a PWM signal for fan control, using the CPU Fan Tach/PWM signal available on the COM-Express connector.

3.14.2 Thermal Monitoring

The system setup utility displays the processor and board temperatures. For further information on how to check these temperatures, refer to *The Haswell Core BIOS Manual.*

3.14.3 Thermal Throttling

3.14.3.1 CPU Throttling (Hardware Controlled)

The processor must not exceed the 100°C maximum junction temperature (Tj).

When the integrated thermal monitor on the processor determines that the maximum processor temperature has been reached, the CPU clock speed will be throttled back in increments to keep Tj from exceeding the maximum junction temperature of 100° C.

If throttling is not enough to keep the processor's Tj below the catastrophic temperature limit of 105° C:

- The THERMATRIP# signal will be sent, and
- The voltage supply to the processor will be turned off within 500ms

to prevent permanent silicon damage.

3.14.3.2 Thermal Management (OSPM Controlled)

The active and passive trip points are configured using the system Bios. For information on how to configure these trip points, refer to *The Haswell Core BIOS Manual.*

3.14.4 Memory Throttling

The memory bandwidth can be throttled back automatically if a thermal sensor is on the DIMM. The NCT6776D will alert the memory controller via PECI when the system memory exceeds its normal operating temperature.

For further information on configuring the memory bandwidth throttling based on temperature readings from the DIMM's thermal sensor, refer to The Haswell Core BIOS Manual.

3.14.5 Thermal Management Hardware

Two types of thermal management hardware are available on the XCOM-6400 for managing and dissipating the thermal energy

generated in the module:

- Heat spreader (standard)
- XHSA-6400 active heat sink (optional)

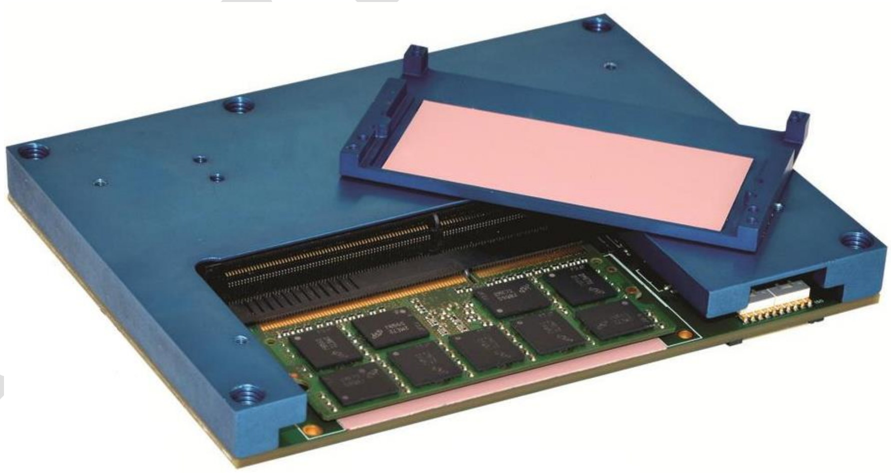
Fig. 3.14.5.a XCOM-6400 without Thermal Management Hardware

This is the XCOM-6400 module without any thermal management hardware attached.



Fig. 3.14.5.b XCOM-6400 and Heat Spreader

This is the XCOM-6400 module with the standard heat spreader installed.

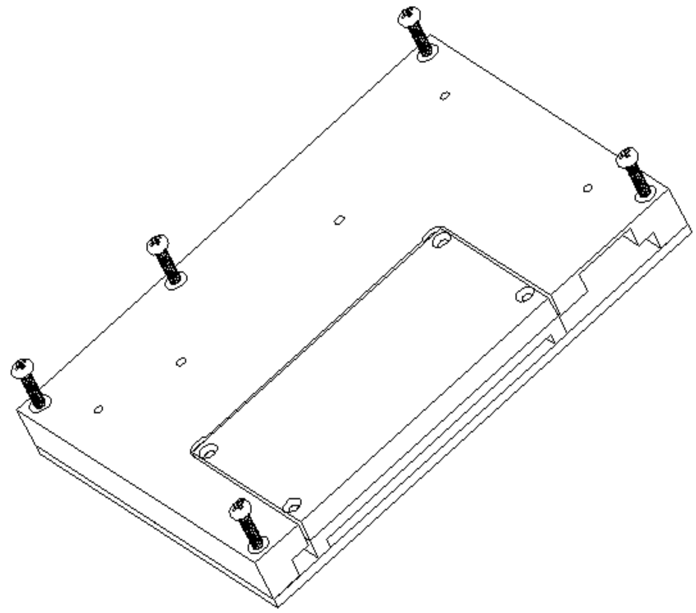


WARNING: Do not attempt to remove the heat spreader.

Once assembled to the XCOM-6400 module, the heat spreader should never need to be removed. The spreader was attached to the CPU via security screws so that the user cannot remove it. Thermal interface material was placed between the CPU and the spreader at the factory, and the module was then tested.

There are M6 threaded mounting holes on the spreader in the five locations per the COM Express specification. These same five holes are also clearance holes for M2.5 x 8mm screws that are to be used to mount the XCOM-6400 to any carrier, as shown in See Fig. 3.1.5.5.e below.

Fig. 3.14.5.c Module Mounting Screw Locations

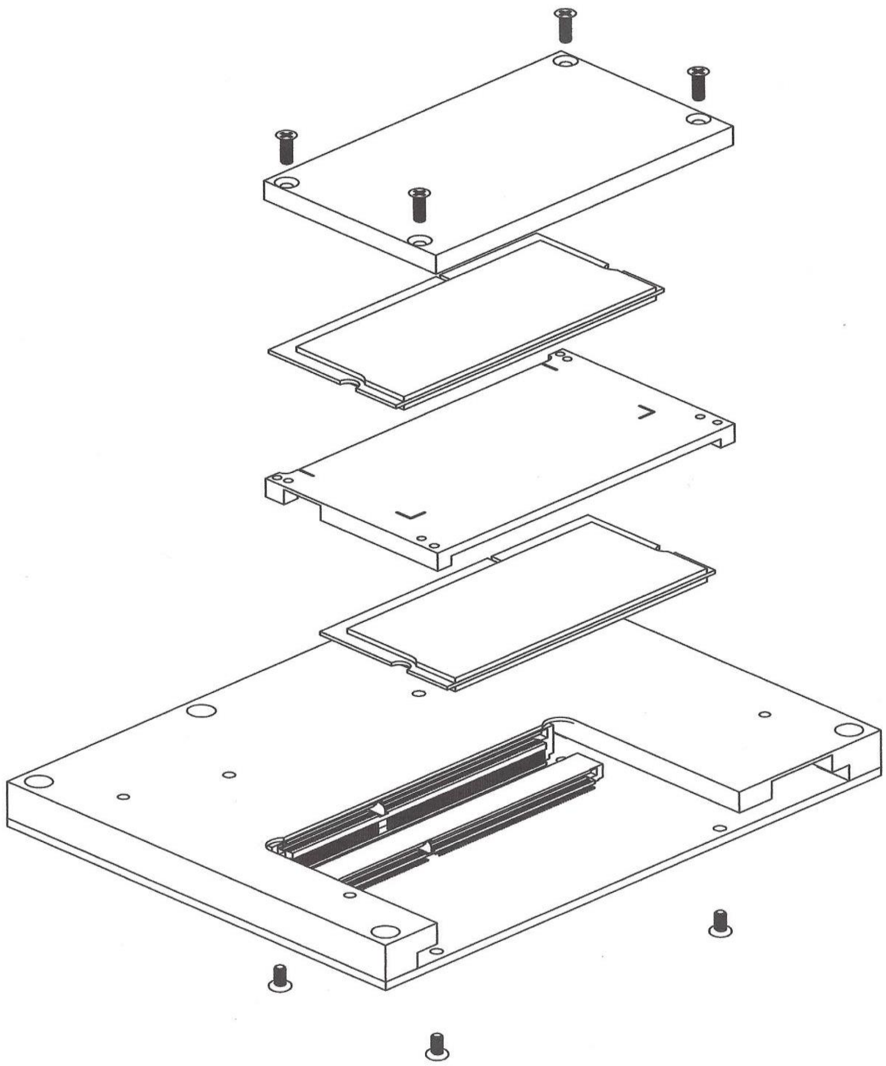


Once the XCOM-6400 has been mounted to a carrier it then can be mounted to any cold plate or enclosure via the M6 threaded holes. The maximum length of the M6 bolt penetration is 0.25 inches.

Note: The maximum M6 bolt penetration is specified to avoid interfering with/contacting the head of the M2.5 screw holding the assembly to the carrier.

Fig. 3.14.5.d SODIMM Assembly

The SODIMM assembly and its components are shown below.



The the XCOM-6400 module with the optional XHSA-6400 active (with fan) heat sink installed is shown below in Fig. 3.15.5.e. The XHSA-6400 would be used in air cooled applications. No thermal grease has been provided with the XHSA-6400. Testing shows that a 5° C improvement at the CPU can be realized if thermal grease or some TIM material is used. The user will be responsible for monitoring the CPU temperature in his/her application and determine if thermal grease is required.

Fig. 3.14.5.e XCOM-6400 with Heat Spreader and Active Heat Sink

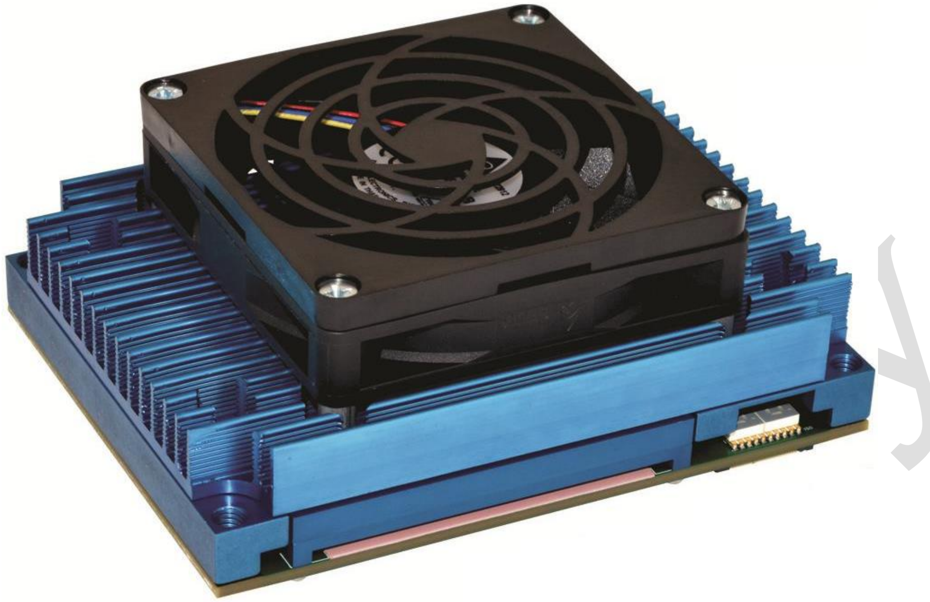


Fig. 3.14.5.f XCOM-6400, ACEX-4620 Carrier Board, and Heat Spreader Assembly

This is the XCOM-6400 module mounted onto the ACEX-4620 carrier board with the standard heat spreader installed.



3.15 Watchdog

The XCOM-6400 features a software-triggered multi-stage watchdog solution. When the watchdog timer expires the WDTO output on the board-to-board interconnects can be configured to go high and/or the module can cause a system reset.

For further information on the Watchdog feature, refer to *The Haswell Core BIOS Manual.*

4.0 BIOS INFORMATION AND CONFIGURATION

4.1 OS Support

This material is still under development.

4.2 Drivers and Utilities

This material is still under development.

5.0 SERVICE AND REPAIR

5.1 Service and Repair Assistance

Single Board Computer (SBC) products like the XCOM-6400 COM Express module are generally difficult to repair. The module can be easily damaged unless special SBC repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. For these and other reasons, it is strongly recommended that a non-functioning SBC be returned to Acromag for repair.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts or return parts for repair.

5.2 Preliminary Service Procedure

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Before beginning repair, be sure that all of the procedures in the "Preparation for Use" section have been followed. Also, refer to the documentation for the module to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

5.3 Where to Get Help

If the problem persists, the next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

Acromag's application engineers can also be contacted directly for technical assistance via email, telephone, or FAX through the contact information listed below. Note that an email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab. When needed, complete repair services are also available.

- Email: solutions@acromag.com
- Phone: 248-624-1541
- Fax: 248-624-9234

6.0 SPECIFICATIONS

6.1 Physical

Height (including PCB thickness)	13.0 mm (0.512 in)
Depth	95.0 mm (3.740 in)
Width	125.0 mm (4.921 in)
Board Thickness	2.49 mm (0.098 in)

Unit Weight (including heat spreader): 11.9 oz (0.337 kg)

6.1.1 J3 Connector

26-pin Molex 52435-2671 connector complies with Intel Shark Bay Debug Port Design Guide.

6.1.2 J4 Connector

440-pin Tyco Electronics 3-1827231-6 connector complies with PICMG COM.0 COM Express Module Base Specification Revision 2.1.

6.2 Power Requirements

The power required to properly operate XCOM-6400 module will vary depending on many variables, including the application and the components that the module is integrated with. Acromag has determined the following typical power requirements for the XCOM-6400 module:

+12VDC (±5%)	Typical TBD	Max. TBD
Optional: +5V Standby (±5%)	Typical TBD	Max. TBD

These power requirements were determined when testing the module with the following components and software:

- Carrier board:
- EDK
- Hard disk:
- Memory:
- Monitor
- Keyboard and mouse:
- Operating system:
- Test software:

6.3 Environmental Considerations

Operating Temperature:

- 0° C to 70° C (Standard temperature model)
- -25°C to 85°C (Extended temperature model)

Note: CPU Tj temperature must not exceed 100°C. This temperature should be monitored in end user system with user application software running to determine if thermal solution is adequate.

Relative Humidity: 5% to 95% Non-condensing

Storage Temperature: -55° C to 100° C

6.4 Certificate of Volatility

Certificate of Volatility				
Acromag Model XCOM-6400-XXXX	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) ■ Yes □ No				
Type (SRAM, SDRAM, etc.) SDRAM	Size: Up to 16GB (depends on SODIMM modules installed)	User Modifiable ■ Yes □ No	Function: Storage of code/data for CPU	Process to Sanitize: Power Down
Type (SRAM, SDRAM, etc.) PCH internal CMOS SRAM	Size: 256 bytes	User Modifiable ■ Yes □ No	Function: Data storage for system/BIOS	Process to Sanitize: Momentarily close switches SW1-3 and SW1-4.
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) ■ Yes □ No				
Type(EEPROM, Flash, etc.) Flash	Size: 16Mbyte	User Modifiable ■ Yes □ No	Function: Storage of Code and Data for system/BIOS	Process to Sanitize: Clear Flash memory by erasing all sectors of the Flash
Type(EEPROM, Flash, etc.) EEPROM	Size: 16Kbyte	User Modifiable ■ Yes □ No	Function: Storage of Module ID and/or User Data	Process to Sanitize: Clear EEPROM memory by erasing all bytes.
Acromag Representative				
Name: Joseph Primeau	Title: Dir. of Sales and Marketing	Email: jprimeau@acromag.com	Office Phone: 248-295-0823	Office Fax: 248-624-9234

6.5 Revision History

Revision	Date (mm/dd/yyyy)	Author	Change Description
A	11/14/2013	DWR/TG	Preliminary release

APPENDIX A: COM EXPRESS CONNECTOR (J4) PINOUT TABLES

Pin	Row A	Row B	Row C	Row D
1	GND	GND	GND	GND
2	GBE0_MDI3-	GBE0_ACT#	GND	GND
3	GBE0_MDI3+	LPC_FRAME#	USB_SSRX0-	USB_SSTX0-
4	GBE0_LINK100#	LPC_AD0	USB_SSRX0+	USB_SSTX0+
5	GBE0_LINK1000#	LPC_AD1	GND	GND
6	GBE0_MDI2-	LPC_AD2	USB_SSRX1-	USB_SSTX1-
7	GBE0_MDI2+	LPC_AD3	USB_SSRX1+	USB_SSTX1+
8	GBE0_LINK#	NO CONNECT[1]	GND	GND
9	GBE0_MDI1-	LPC_DRQ1#	USB_SSRX2-	USB_SSTX2-
10	GBE0_MDI1+	LPC_CLK	USB_SSRX2+	USB_SSTX2+
11	GND	GND	GND	GND
12	GBE0_MDI0-	PWRBTN#	USB_SSRX3-	USB_SSTX3-
13	GBE0_MDI0+	SMB_CK	USB_SSRX3+	USB_SSTX3+
14	NO CONNECT	SMB_DAT	GND	GND
15	SUS_S3#	SMBALERT#	NO CONNECT[1]	DDI1_CTRLCLK_AUX+
16	SATA0_TX+	SATA1_TX+	NO CONNECT[1]	DDI1_CTRLDATA_AUX-
17	SATA0_TX-	SATA1_TX-	NO CONNECT	NO CONNECT
18	SUS_S4#	SUS_STAT#	NO CONNECT	NO CONNECT
19	SATA0_RX+	SATA1_RX+	PCIE_RX6+	PCIE_TX6+
20	SATA0_RX-	SATA1_RX-	PCIE_RX6-	PCIE_TX6-
21	GND	GND	GND	GND
22	SATA2_TX+	SATA3_TX+	NO CONNECT[1]	NO CONNECT[1]
23	SATA2_TX-	SATA3_TX-	NO CONNECT[1]	NO CONNECT[1]
24	SUS_S5#	PWR_OK	DDI1 HPD	NO CONNECT
25	SATA2_RX+	SATA3_RX+	NO CONNECT[1]	NO CONNECT
26	SATA2_RX-	SATA3_RX-	NO CONNECT[1]	DDI1_PAIR0+
27	BATLOW#	WDT	NO CONNECT	DDI1_PAIR0-
28	SATA_ACT#	HAD_SDIN2	NO CONNECT	NO CONNECT
29	HAD_SYNC	HAD_SDIN1	NO CONNECT[1]	DDI1_PAIR1+
30	HAD_RST#	HAD_SDIN0	NO CONNECT[1]	DDI1_PAIR1-
31	GND	GND	GND	GND
32	HDA_BITCLK	SPKR	DDI2_CTRLCLK_AUX+	DDI1_PAIR2+
33	HDA_SDOUT	I^2C_CK	DDI2_CTRLDATA_AUX-	DDI1_PAIR2-
34	NO CONNECT[1]	1^2C_DAT	DDI2_DDC_AUX_SEL	DDI1_DDC_AUX_SEL
35	THRMTRIP#	THRM#	NO CONNECT	NO CONNECT
36	USB6-	USB7-	DDI3_CTRLCLK_AUX+	DDI1_PAIR3+
37	USB6+	USB7+	DDI3_CTRLDATA_AUX-	DDI1_PAIR3-
38	USB_6_7_OC#	USB_4_5_OC#	DDI3_DDC_AUX_SEL	NO CONNECT
39	USB4-	USB5-	DDI3_PAIR0+	DDI2_PAIR0+
40	USB4+	USB5+	DDI3_PAIR0-	DDI2_PAIR0-
41	GND	GND	GND	GND
42	USB2-	USB3-	DDI3_PAIR1+	DDI2_PAIR1+
43	USB2+	USB3+	DDI3_PAIR1-	D012_PAIR1-

Pin	Row A	Row B	Row C	Row D
44	USB_2_3_OC#	USB_0_1_OC#	DDI3_HPD	DDI2_HPD
45	USB0-	USB1-	NO CONNECT	NO CONNECT
46	USB0+	USB1+	DDI3_PAIR2+	DDI2_PAIR2+
47	VCC_RTC	NO CONNECT[1]	DDI3_PAIR2-	DDI2_PAIR2-
48	NO CONNECT[1]	NO CONNECT[1]	NO CONNECT	NO CONNECT
49	NO CONNECT[1]	SYS_RESET#	DDI3_PAIR3+	DDI2_PAIR3+
50	LPC_SERIRQ	CB_RESET#	D013_PAIR3-	DDI2_PAIR3-
51	GND	GND	GND	GND
52	PCIE_TX5+	PCIE_RX5+	PEG_RX0+	PEG_TX0+
53	PCIE_TX5-	PCIE_RX5-	PEG_ RX0-	PEG_ TX0-
54	GPI0	GPO1	TYPE0# (NO CONNECT)	PEG_ LANE_RV#
55	PCIE_TX4+	PCIE_RX4+	PEG_ RX1+	PEG_ TX1+
56	PCIE_TX4-	PCIE_RX4-	PEG_ RX1-	PEG_ TX1-
57	GND	GPO2	TYPE1# (NO CONNECT)	TYPE2# (GND)
58	PCIE_TX3+	PCIE_RX3+	PEG_ RX2+	PEG_ TX2+
59	PCIE_TX3-	PCIE_RX3-	PEG_ RX2-	PEG_ TX2-
60	GND	GND	GND	GND
61	PCIE_TX2+	PCIE_RX2+	PEG_ RX3+	PEG_ TX3+
62	PCIE_TX2-	PCIE_RX2-	PEG_ RX3-	PEG_ TX3-
63	GPI1	GPO3	NO CONNECT	NO CONNECT
64	PCIE_TX1+	PCIE_RX1+	NO CONNECT	NO CONNECT
65	PCIE_TX1-	PCIE_RX1-	PEG_ RX4+	PEG_TX4+
66	GND	WAKE0#	PEG_ RX4-	PEG_TX4-
67	GPI2	WAKE1#	NO CONNECT	GND
68	PCIE_TX0+	PCIE_RX0+	PEG_ RX5+	PEG_TX5+
69	PCIE_TX0-	PCIE_RX0-	PEG_ RX5-	PEG_TX5-
70	GND	GND	GND	GND
71	NO CONNECT	NO CONNECT[1]	PEG_ RX6+	PEG_TX6+
72	NO CONNECT	NO CONNECT[1]	PEG_ RX6-	PEG_TX6-
73	eDP_TX1+	NO CONNECT[1]	GND	GND
74	eDP_TX1-	NO CONNECT[1]	PEG_ RX7+	PEG_TX7+
75	eDP_TX0+	NO CONNECT[1]	PEG_ RX7-	PEG_TX7-
76	eDP_TX0-	NO CONNECT[1]	GND	GND
77	eDP_VDD_EN	NO CONNECT[1]	NO CONNECT	NO CONNECT
78	NO CONNECT	NO CONNECT[1]	PEG_RX8+	PEG_TX8+
79	NO CONNECT	eDP_BKLT_EN	PEG_RX8-	PEG_TX8-
80	GND	GND	GND	GND
81	NO CONNECT	NO CONNECT[1]	PEG_RX9+	PEG_TX9+
82	NO CONNECT	NO CONNECT[1]	PEG_RX9-	PEG_TX9-
83	eDP_AUX+	eDP_BKLT_CTRL	NO CONNECT	NO CONNECT
84	eDP_AUX-	VCC_5V_SBY	GND	GND
85	GPI3	VCC_5V_SBY	PEG_RX10+	PEG_TX10+
86	NO CONNECT	VCC_5V_SBY	PEG_RX10-	PEG_TX10-
87	eDP_HPD	VCC_5V_SBY	GND	GND
88	PCIE_CLK_REF	NO CONNECT[1]	PEG_RX11+	PEG_TX11+
89	PCIE_CLK_REF	VGA_RED	PEG_RX11-	PEG_TX11-
90	GND	GND	GND	GND

Pin	Row A	Row B	Row C	Row D
91	SPI_POWER	VGA_GRN	PEG_RX12+	PEG_TX12+
92	SPI_MISO	VGA_BLU	PEG_RX12-	PEG_TX12-
93	GPO0	VGA_HSYNC	GND	GND
94	SPI_CLK	VGA_VSYNC	PEG_RX13+	PEG_TX13+
95	SPI_MOSI	VGA_I^{2}C_CK	PEG_RX13-	PEG_TX13-
96	NO CONNECT[1]	VGA_I^{2}C_DAT	GND	GND
97	TYPE10# (NO CONNECT)	SPI_CS1#	NO CONNECT	NO CONNECT
98	SER0_TX	NO CONNECT	PEG_RX14+	PEG_TX14+
99	SER0_RX	NO CONNECT	PEG_RX14-	PEG_TX14-
100	GND	GND	GND	GND
101	SER1_TX	FAN_PWMOUT	PEG_RX15+	PEG_TX15+
102	SER1_RX	FAN_TACHIN	PEG_RX15-	PEG_TX15-
103	NO CONNECT[1]	NO CONNECT[1]	GND	GND
104	VCC_12V	VCC_12V	VCC_12V	VCC_12V
105	VCC_12V	VCC_12V	VCC_12V	VCC_12V
106	VCC_12V	VCC_12V	VCC_12V	VCC_12V
107	VCC_12V	VCC_12V	VCC_12V	VCC_12V
108	VCC_12V	VCC_12V	VCC_12V	VCC_12V
109	VCC_12V	VCC_12V	VCC_12V	VCC_12V
110	GND	GND	GND	GND

For detailed signal descriptions, refer to the COM-Express Module Base Specification Rev. 2.1

Note 1: The functionality of the signals on these pins as described in the COM Express Module Base Specification Rev. 2.1 is not available on the XCOM-6400 module.